

DAFTAR PUSTAKA

- Ali, M. S. (2018). Cascaded ripple carry adder based SRCSA for efficient FIR filter. *Indonesian Journal of Electrical Engineering and Computer Science*, 9(2), 253–256. <https://doi.org/10.11591/ijeecs.v9.i2.pp253-256>
- Alkurwy, S. H., & Hameed, I. S. (2022). A novel pipelined carry adder design based on half adder. *Indonesian Journal of Electrical Engineering and Computer Science*. <https://doi.org/10.11591/ijeecs.v25.i2.pp763-770>
- Bedir, N. S., & Kaçar, F. (2019). Design and simulation of 64 bit FPGA based arithmetic logic unit. *Electrica*, 19(2), 158–165. <https://doi.org/10.26650/electrica.2019.18052>
- Borodzhieva, A. N., Stoev, I. I., & Mutkov, V. A. (2019). FPGA implementation of boolean functions using multiplexers. *2019 28th International Scientific Conference Electronics, ET 2019 - Proceedings*. <https://doi.org/10.1109/ET.2019.8878504>
- Borodzhieva, A., Stoev, I., & Mutkov, V. (2019a). Application of Active Learning Methods in the Course “digital Electronics” in the Topic Digital Comparators Using FPGA Design. *SIITME 2019 - 2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging, Proceedings, October 2019*, 160–163. <https://doi.org/10.1109/SIITME47687.2019.8990786>
- Borodzhieva, A., Stoev, I., & Mutkov, V. (2019b). FPGA Implementation of Boolean Functions Using Decoders and Logic Gates. *SIITME 2019 - 2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging, Proceedings, October*, 164–167. <https://doi.org/10.1109/SIITME47687.2019.8990690>
- Dermawan, D., Putra, M. A. M., Waluyo, C. B., & Sudibya, B. (2020). Rancang Bangun Arithmetic Logic Unit 8 Bit Pada Spartan 2 Field Programmable Gate Array. *Conference SENATIK STT Adisutjipto Yogyakarta*, 6, 185–198. <https://doi.org/10.28989/senatik.v6i0.423>
- Friendly. (2017). Perancangan Mikroprosesor 8 Bit Dengan Menggunakan Bahasa VHDL pada FPGA Xilinx Spartan 3. *Teknovasi*, 4(1), 10–27.

- Hutagaol, D. (2013). *Pengantar Penerbangan Perspektif Profesional*. Penerbit Erlangga.
- Jaafar, A., Soin, N., & Hatta, S. W. M. (2017). An educational FPGA design process flow using Xilinx ISE 13.3 project navigator for students. *Proceedings - 2017 IEEE 13th International Colloquium on Signal Processing and Its Applications, CSPA 2017, March*, 7–12.
<https://doi.org/10.1109/CSPA.2017.8064915>
- Kurniawan, F. (2018). *Diktat Teknik Digital* (ketiga). Sekolah Tinggi Teknologi Adisutjipto Yogyakarta.
- Nangia, R., & Shukla, N. K. (2018). Resource Utilization Optimization with Design Alternatives in FPGA based Arithmetic Logic Unit Architectures. *Procedia Computer Science*, 132, 843–848. <https://doi.org/10.1016/j.procs.2018.05.096>
- Pattnaik, S. K., Nanda, U., Nayak, D., Mohapatra, S. R., Nayak, A. B., & Mallick, A. (2018). Design and implementation of different types of full adders in ALU and leakage minimization. *Proceedings - International Conference on Trends in Electronics and Informatics, ICEI 2017, 2018-Janua*, 924–927.
<https://doi.org/10.1109/ICOEI.2017.8300841>
- Rani, A., & Grover, N. (2018). An enhanced FPGA based asynchronous microprocessor design using VIVADO and ISIM. *Bulletin of Electrical Engineering and Informatics*, 7(2), 199–208.
<https://doi.org/10.11591/eei.v7i2.818>
- Saravanakumar, S., Vijeyakumar, V., & Sakthisudhan, S. (2018). FPGA Implementation of High Speed Hardware Efficient Carry Select Adder. *International Journal of Reconfigurable and Embedded Systems (IJRES)*, 7(1), 43. <https://doi.org/10.11591/ijres.v7.i1.pp43-47>
- Shylaja, C., Rai, A., & Mishra, P. K. (2021). Modelling and Simulation of 16-bit Vedic Multiplication Using FPGA. *Journal of Physics: Conference Series*.
<https://doi.org/10.1088/1742-6596/2007/1/012003>
- Suryawan, F. (2017). A project-based approach to FPGA-aided teaching of digital systems. *International Conference on Electrical Engineering, Computer Science and Informatics (EECSI), 2017-Decem(September)*, 19–21.
<https://doi.org/10.1109/EECSI.2017.8239177>

- Swamynathan, S. M., & Banumathi, V. (2017). Design and analysis of FPGA based 32 bit ALU using reversible gates. *Proceedings - 2017 IEEE International Conference on Electrical, Instrumentation and Communication Engineering, ICEICE 2017, 2017-Decem*(April 2017), 1–4.
<https://doi.org/10.1109/ICEICE.2017.8191959>
- Swathi, V., Panduga, K., & Kumari, G. S. (2021). Design of High Performance ALU Using Vedic Mathematics. *Journal of Physics: Conference Series*.
<https://doi.org/10.1088/1742-6596/1964/6/062031>
- Thabah, S. D., Sonowal, M., & Saha, P. (2017). *EXPERIMENTAL STUDIES ON MULTI-OPERAND ADDERS*. 10(2), 327–340.
- Thakral, S., & Bansal, D. (2020). High functionality reversible arithmetic logic unit. *International Journal of Electrical and Computer Engineering*.
<https://doi.org/10.11591/ijece.v10i3.pp2329-2335>
- Wang, H., & Chen, X. (2019). Development and Optimization Design of Digital Logic device based on FPGA. *Journal of Physics: Conference Series*, 1345(6).
<https://doi.org/10.1088/1742-6596/1345/6/062051>
- Yadav, N., & Kumari, P. (2018). Design of ALU using dual mode logic with optimized power and speed. *IMPACT 2017 - International Conference on Multimedia, Signal Processing and Communication Technologies*, 41–45.
<https://doi.org/10.1109/MSPCT.2017.8363970>
- Military Factory - Global Defense Reference*. (2023). Militaryfactory.com.
<https://www.militaryfactory.com/>